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TROP, PRUNER & HU, P.C. 1616 S. VOSS RD., SUITE 750 HOUSTON, TX 77057-2631			MALZAHN, DAVID H	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YEN-KUANG CHEN and MINERVA M. YEUNG

Appeal 2009-013261
Application 10/687,953
Technology Center 2100

Before, ROBERT E. NAPPI, DAVID M. KOHUT, and
MICHAEL R. ZECHER, *Administrative Patent Judges*.

Per Curiam.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) of the final rejection of claims 1-8 and 10-18.¹ We have jurisdiction under 35 U.S.C. § 6(b).

We affirm the Examiner's rejection of these claims.

¹ Claims 9 and 19-29 have been indicated by the Examiner as containing allowable subject matter. Final Rej. 3.

INVENTION

The invention is directed to a machine-accessible medium and method for performing, in a processor, motion compensation and bi-linear interpretation on packed data. Abstract. Claim 1 is representative of the invention and is reproduced below:

1. A method for performing bi-linear interpolation or a motion compensation of a digital image or video, the method comprising:
 - decoding a first shuffle instruction and a first multiply-add instruction, each of an instruction format comprising a first operand field and a second operand field;
 - responsive at least in part to said first shuffle instruction, generating a first packed data having a first plurality of byte data elements including an a_1 byte data element, and at least two copies of each of a_2 , a_3 , and a_4 byte data elements; and
 - responsive to said first multiply-add instruction, wherein the first operand field of said first multiply-add instruction specifies said first packed data and the second operand field specifies a second packed data having a second plurality of byte data elements including at least two copies of each of b_1 and b_2 byte data elements, performing an operation $(a_1 \times b_1) + (a_2 \times b_2)$ to generate a first 16-bit data element of a third packed data, performing an operation $(a_2 \times b_1) + (a_3 \times b_2)$ to generate a second 16-bit data element of the third packed data, and performing an operation $(a_3 \times b_1) + (a_4 \times b_2)$ to generate a third 16-bit data element of the third packed data.

REJECTION AT ISSUE

Claims 1-8 and 10-18 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Ans. 2-4.

ISSUE

Did the Examiner err in finding that claims 1-8 and 10-18 are directed to non-statutory subject matter?

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' contentions that the Examiner has erred. Further, we have reviewed the Examiner's response to each of the independent claims argued.

We disagree with Appellants' conclusions. We adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken and (2) the reasons set forth by the Examiner in the Examiner's rejection of the claims and in the Examiner's Answer in response to Appellants' Appeal Brief. We concur with the conclusions reached by the Examiner.

Additionally, we note that the claims recite an algorithm to produce interpolated data or motion compensation. As indicated by the Examiner on page 3 of the Answer, the claims recite no specific environment in which the interpolation or motion compensation is performed nor are the claims directed to a particular machine to perform the interpolation or motion compensation. Thus, we consider the claims to wholly preempt all uses of the algorithm.

CONCLUSION

The Examiner did not err in finding that claims 1-8 and 10-18 are directed to non-statutory subject matter.

SUMMARY

The Examiner's decision to reject claims 1-8 and 10-18 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

Appeal 2009-013261
Application 10/687,953

AFFIRMED

ELD